VLSI Circuit Design

Code: EE-412

Credit hours: 3-0

Pre-req: None

Course: Elective

Contact hours: 3 Hours (3 Lectures) per week **Text Book:**

1. Digital Integrated Circuits: A Design Perspective by Jan Rabaey, Anantha Chandrakasan & Borivoje Nikolic, 2nd Edition, 2003, Prentice-Hall

Reference Book:

1. Principles of CMOS VLSI Design. N. Weste and D. Harris., 3rd Edition, 2005. Addison Wesley

Prerequisite: Nill

Mode of teaching: Lectures

Course Description:- This course aims at providing the under-graduate electronic engineering students an introduction to integrated circuits, IC fabrication process, VLSI circuits and systems and their design. The main focus of this course is the study of basic electrical properties of CMOS, design of basic digital building blocks using MOS transistors, modeling of interconnecting wires and clocking techniques. The course also addresses the optimization of designs with respect to a number of metrics: cost, reliability, performance, and power dissipation. The course objective is to provide the student with a solid understanding of the underlying mechanism and solution techniques to the above design issues, so that the student, when working as industrial designer, is capable of identifying the key problems and focus his attention to resolve them. The students will learn to use Cadence ASIC Design Suite during the course.

Course Objectives:

By the end of the course the students will be able to:

Describe VLSI systems and list specific examples.

- Analyze the operation of CMOS inverter characterize its performance.
- Analyze the operation of various CMOS based logic functions.
- Design and simulate transistor based digital circuits.

- Create layouts for fabrication of ASICs.
- Analyze and design various types of memories.
- Use Cadence software to simulate and design ASICs

Topics Covered:

Introduction

- Historical Perspective
- Design metrics
- IC Manufacturing and Design Rules
- Switch Logic
- Complex Logic
- Inverter Delay Optimization
- Logical Effort
- Logical Effort / Memory
- Wires
- MOS transistor model
- MOS transistor + Capacitance
- MOS Capacitance + VTC
- CMOS Delay model
- CMOS power
- Technology Scaling
- Complex Logic Optimization
- Pass Transistor Logic
- Dynamic Logic
- Energy/Power
- Memory
- Latches/Registers
- Sequential Logic
- Timing
- Clocks and Power
- Arithmetic

Course Targets:

	Course Learning Outcome (CLOs)	**PLOs**	**Learning Level**
CLO 1	ANALYSE mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnects	1	C3
CLO 2	APPLY CMOS technology-specific layout rules in the placement and routing of transistors and interconnects, and to verify the functionality, timing, power, and parasitic effects.	2	C3
CLO 3	DESIGN all the key steps involved in device/circuit designing starting from scratch to the final design files in acceptable format.	3	C6